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EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2111	8

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/940,292	CRETA ET AL.	
	Examin r	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6&7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected based on lack of positive antecedent basis of "the outbound transactions transmitted from an unordered protocol."

Claims 2-4 are rejected because they depend on claim 1.

Claim 4 is also rejected based on lack of positive antecedent basis of "the coherent interface" on line 1.

Claim 5 is rejected based on lack of positive antecedent basis of "the outbound transactions from the unordered protocol" on lines 22-23.

Claims 6-11 are rejected because they depend on claim 5.

Claim 11 is also rejected based on lack of positive antecedent basis of "the coherent interface" on line 1.

Claim 12 is rejected based on lack of positive antecedent basis of "the outbound transactions from the unordered protocol" on lines 22-23.

Claims 13-15 are rejected because they depend on claim 12.

Claim 16 is rejected based on lack of positive antecedent basis of "the outbound transactions from the unordered protocol" on lines 22-23.

Claims 17-21 are rejected because they depend on claim 16.

Claim 22 is rejected based on lack of positive antecedent basis of "the outbound transactions from the coherent interface" on line 25.

Claims 23-25 are rejected because they depend on claim 22.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,5-10,12,14-16, and 18-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Neal et al., European Patent Application EP 0 747 831 A2 (cited by applicant).

As per claim 1, Neal et al. (Neal) shows an inbound ordering queue (IOQ) to receive inbound transactions (fig.2,224,226,228), wherein all read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination (throughout cols 3-7); an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ (fig.2,232,234); an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write (fig.2,210,212,214 and in cols. 3-7); an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ (216,218); and an unordered domain to receive the inbound

transactions transmitted from the IOQ and to receive the outbound transactions transmitted from an unordered protocol (cols. 3-7). Neal shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Neal also shows that the IOQ does not permit the inbound read and write transactions to bypass inbound write data (col.7). Neal shows all of the elements recited in claim 2.

As for claim 3, the argument for claim 1 applies. Neal also shows that the unordered protocol is a coherence interface (throughout the discussion of the system operation in cols. 3-7). Neal shows all of the elements recited in claim 3.

As per claim 5, Neal shows an ordered domain, including: an inbound ordering queue (IOQ) to receive and transmit inbound transactions (as above, fig.2,224,226,228), wherein inbound read and write transactions are not permitted to bypass inbound write data, all the read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination (cols. 3-7); an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ (232,234); an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write (210,212,214 and cols. 3-7); and an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ (216,218); and an unordered domain, in communication with an unordered protocol, including: an inbound multiplexer to receive the inbound transactions from the ordered domain to the unordered protocol (230), and an

outbound demultiplexer to receive the outbound transactions from the unordered protocol to the ordered domain (208). Neal shows all of the elements recited in claim 5.

As for claim 6, the argument for claim 5 applies. Neal also shows at least one Producer-Consumer ordered interface in communication with the ordered domain (inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E). Neal shows all of the elements recited in claim 6.

As for claim 7, the argument for claim 6 applies. Neal also shows an input/output device connected with the Producer-Consumer ordered interface (fig.1, (30,40) and inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E). Neal shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 7 applies. Neal also shows an intermediary device interconnecting the Producer-Consumer ordered interface and an input/output device (inside bridge 20 and as in fig.2). Neal shows all of the elements recited in claim 8.

As for claim 9, the argument for claim 7 applies. Neal also shows that the input/output device is a Peripheral Component Interconnect (PCI) device (at least in cols. 1-2). Neal shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 5 applies. Neal also shows that the unordered protocol is a coherence interface (throughout the discussion of the system operation in cols. 3-7). Neal shows all of the elements recited in claim 10.

As per claim 12, Neal shows an ordered domain, including: an inbound ordering queue (IOQ) to receive and transmit inbound transactions (as above, fig.2,224,226,228), wherein inbound read and write transactions are not permitted to bypass inbound write data, all the read

and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination (cols. 3-7); an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ (232,234); an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write (210,212,214 and cols. 3-7); and an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ (216,218); and an unordered domain, in communication with an unordered protocol, including: an inbound multiplexer to receive the inbound transactions from the ordered domain to the unordered protocol (230), and an outbound demultiplexer to receive the outbound transactions from the unordered protocol to the ordered domain (208); a Producer-Consumer ordered interface in communication with the ordered domain (inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E); an input/output device connected with the Producer-Consumer ordered interface (fig.1, (30,40) and inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E); and a coherent interface within the unordered protocol in communication with the unordered domain (cols. 3-7). Neal shows all of the elements recited in claim 12.

As for claim 14, the argument for claim 12 applies. Neal also shows that the input/output device is a Peripheral Component Interconnect (PCI) device (at least in cols. 1-2). Neal shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 12 applies. Neal also shows an intermediary device interconnecting the Producer-Consumer ordered interface and an input/output device (inside bridge 20 and as in fig.2). Neal shows all of the elements recited in claim 15.

As per claim 16, Neal shows an ordered domain, including: an inbound ordering queue (IOQ) to receive and transmit inbound transactions (as above, fig.2,224,226,228), wherein inbound read and write transactions are not permitted to bypass inbound write data, all the read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination (cols. 3-7); an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ (232,234); an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write (210,212,214 and cols. 3-7); and an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ (216,218); and an unordered domain, in communication with an unordered protocol, including: an inbound multiplexer to receive the inbound transactions from the ordered domain to the unordered protocol (230), and an outbound demultiplexer to receive the outbound transactions from the unordered protocol to the ordered domain (208); a first Producer-Consumer ordered interface in communication with the first functional block (inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E); a first input/output device connected with the first Producer-Consumer ordered interface (fig.1, (30,40) and inherent in that Neal is for use in a PCI system and the PCI specification version 2.1

as provided by applicant outlines the producer-consumer ordering in Appendix E); a second Producer-Consumer ordered interface in communication with the second functional block (inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E); a second input/output device connected with the second Producer-Consumer ordered interface fig.1, (30,40) and inherent in that Neal is for use in a PCI system and the PCI specification version 2.1 as provided by applicant outlines the producer-consumer ordering in Appendix E); and a coherent interface within the unordered protocol in communication with the unordered domain (cols. 3-7). Neal shows all of the elements recited in claim 16.

As for claim 18, the argument for claim 16 applies. Neal also shows that the first input/output device is a Peripheral Component Interconnect (PCI) device (at least in cols. 1-2). Neal shows all of the elements recited in claim 18.

As for claim 19, the argument for claim 16 applies. Neal also shows that the second input/output device is a Peripheral Component Interconnect (PCI) device (at least in cols. 1-2). Neal shows all of the elements recited in claim 19.

As for claim 20, the argument for claim 16 applies. Neal also shows a first intermediary device interconnecting the first Producer-Consumer ordered interface and a first input/output device (inside bridge 20 and as in fig.2). Neal shows all of the elements recited in claim 20.

As for claim 21, the argument for claim 16 applies. Neal also shows a second intermediary device interconnecting the second Producer-Consumer ordered interface and a second input/output device (inside bridge 20 and as in fig.2). Neal shows all of the elements recited in claim 21.

As per claim 22, Neal shows a plurality of processor units having access to caches (12); a main memory (inherent in such a computer system); a coherent interface to maintain

coherency between the processor units and their caches (cols. 3-7); a scalability node controller interconnecting the processor units, the main memory, and the coherent interface to control interface therebetween (20); and an input/output hub (20) in communication with the coherent interface, including: an inbound ordering queue (IOQ) to receive inbound transactions, wherein all read and write transactions have a transaction completion, peer-to-peer transactions are not permitted to reach a destination until after all prior writes in the IOQ have been completed, and a write in a peer-to-peer transaction does not permit subsequent accesses to proceed until the write is guaranteed to be in an ordered domain of the destination (in fig.2 as noted in the claims above an in cols. 3-7); an IOQ read bypass buffer to receive read transactions pushed from the IOQ to permit posted writes and read/write completions to progress through the IOQ (in fig.2 as noted above); an outbound ordering queue (OOQ) to store outbound transactions and completions of the inbound transactions, and to issue a write completion for a posted write (fig.2); an OOQ read bypass buffer to receive read transactions pushed from the OOQ to permit the posted writes and the read/write completions to progress through the OOQ (fig.2); and an unordered domain to receive the inbound transactions transmitted from the IOQ and to receive the outbound transactions from the coherent interface (cols. 3-7). Neal shows all of the elements recited in claim 22.

As for claim 23, the argument for claim 22 applies. Neal also shows that the IOQ does not permit the inbound read and write transactions to bypass inbound write data (col.7). Neal shows all of the elements recited in claim 23.

As for claim 24, the argument for claim 22 applies. Neal also shows that the unordered protocol is a coherence interface (throughout the discussion of the system operation in cols. 3-7). Neal shows all of the elements recited in claim 24.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 4,11,13,17, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neal in view of Cataldo, "Intel Prepares for Server Chip Set Revival", EE Times, August 23, 2001 (cited by applicant).

As per claims 4,11,13,17, and 25, Neal does not specifically show that the coherent interface is a Scalability Port. However, Cataldo shows the use of scalability port switching devices for linking processing nodes and an I/O hub that connects to system buses. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the coherent interface of Neal as a scalability port as shown by Cataldo in order to link to multiple processors and the I/O hub circuitry.

Conclusi n

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited reference shows transaction ordering using inbound and outbound queues in a bridge.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
February 5, 2004